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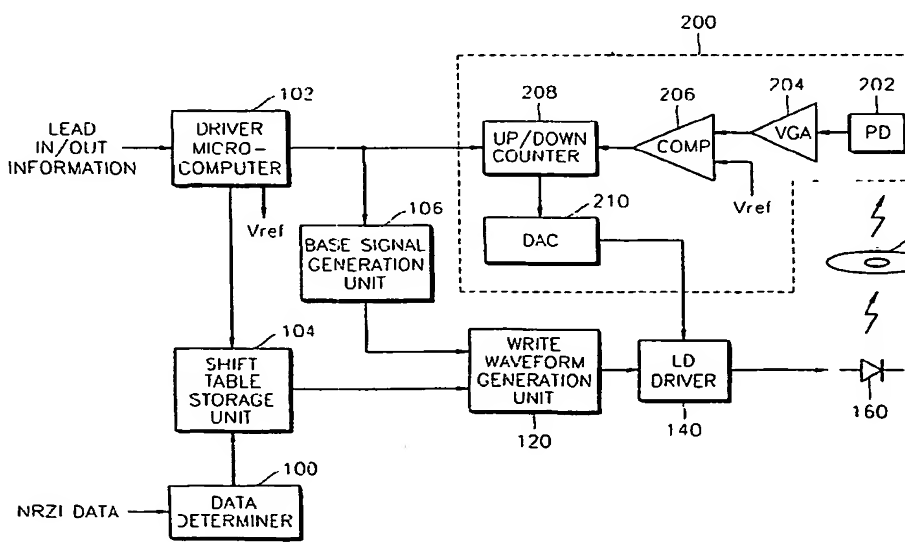
(54) **Method of generating write pulse control signals for optical recording media, and recording apparatus adopting the same**

(57) A method of generating write pulse control signals adaptive to various optical recording media, and a recording apparatus adopting the method. Timing data is obtained with respect to starting and/or ending positions of pulses, relative to rising and falling edges of a mark, wherein the timing data includes a first pulse, a multi-pulse train, a last pulse and a cooling pulse, and the starting and ending positions of the pulses are varied for various optical recording media. The timing data is stored (102), and then a bias power control signal, an erase power control signal, a peak power control signal and a cooling power control signal are generated (120) in synchronism with an input nonreturn to zero inverted (NRZI) signal, based on the timing data for each optical recording medium. The recording apparatus can store write pulses, which are adaptive to various optical recording media, in the form of timing data, and generate (106) base signals based on the timing data. Also, the write pulse control signals can be generated (120) by the base signals, which controls timing of the write pulses such that the optical recording can be realized adaptive to various optical recording media.

FIG. 6



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Description

[0001] The present invention relates to a method and apparatus for high density optical recording, and more particularly, to a method of generating write pulse control signals adaptive to various optical recording media, and a recording apparatus adopting the same.

[0002] With the advent of multimedia, the demand for high capacity recording media has increased. Such high-capacity recording media include digital versatile disk-random access memory (DVD-RAM), DVD-recordable (DVD-R), DVD-rewritable (DVD-RW), DVD+RW and compact disc-RW (CD-RW).

[0003] An ideal optical disc recording apparatus is one that can read or write information from or to various optical recording media such as DVD-RAM, DVD-R, DVD-RW, DVD+RW and CD-RW. However, due to different recording characteristics between optical recording media, the type of write pulse also differs depending on the type of recording media. For this reason, in order to record data on various types of optical recording media, an optical disc recording apparatus must include a plurality of apparatus, each of which is individually available for use with a specific optical recording medium, capable of generating various write pulses. Thus, the amount of hardware becomes excessive.

[0004] An aim of the present invention is to provide a method for generating a write pulse control signal suitable for various optical recording media.

[0005] Another aim of the present invention is to provide a recording apparatus adopting the write pulse control signal generating method.

[0006] According to the present invention there is provided a method for generating write pulse control signals as set forth in claim 1 appended hereto. Also according to the present invention there is provided a recording apparatus which is adaptive to various optical recording media, as set forth in claim 8 appended hereto. Preferred features of the present invention will be apparent from the dependent claims and the description which follows.

[0007] According to a first aspect of the present invention there is provided a method for generating write pulse control signals which are adaptive to various optical recording media, the method comprising the steps of: (a) making timing data with respect to starting and/or ending positions of pulses, relative to rising and falling edges of a mark, wherein the timing data comprises a first pulse, a multi-pulse train, a last pulse and a cooling pulse, and the starting and ending positions of the pulses are varied for various optical recording media; (b) storing the timing data from the step (a); and (c) generating a bias power control signal, an erase power control signal, a peak power control signal and a cooling power control signal in synchronism with an input nonreturn to zero inverted (NRZI) signal, based on the timing data for each optical recording medium.

[0008] Preferably, the timing data obtained in the step (a) are for the starting and ending positions of the first pulse, the starting position of the multi-pulse train, the starting and ending positions of the last pulse, and the ending position of the cooling pulse are made into the timing data.

[0009] Preferably, a first base point for the timing data which represent the starting and ending positions of the first pulse and the starting position of the multi-pulse train is a rising edge of the mark, and a second base point for the timing data which represent the starting and ending position of the last pulse and the ending position of the cooling pulse is a falling edge of the mark.

[0010] Preferably, the first base point for the timing data which represent the starting and ending positions of the last pulse and the starting position of the multi-pulse train precedes the rising edge of the mark by 1T, and the second base point for the timing data which represent the starting and ending position of the last pulse and the ending position of the cooling pulse precedes the falling edge of the mark by 3T, where "T" is a cycle of a reference clock for each optical recording medium.

[0011] Preferably, the starting and ending positions of the first pulse and the starting position of the multi-pulse train are set to be one of a plurality of setting points for each position, the setting points being spaced apart by an equal interval from the first base point, and the starting and ending positions of the last pulse and the ending position of the cooling pulse are set to be one of a plurality of setting points for each position, the setting points being spaced apart by an equal interval from the second base point.

[0012] Preferably, the step (c) comprises the sub-steps of (c1) generating base signals including a first pulse start signal, a first pulse end signal, a multi-pulse start signal, an erase power control signal, a last pulse start signal, a last pulse end signal and a cooling pulse end signal, which are based on the timing data for each optical recording medium; and (c2) generating a bias power control signal, an erase power control signal, a peak power control signal and a cooling power control signal in response to the base signals.

[0013] Preferably, the method further comprises the steps of (d) determining variations of the pulses in a time domain according to a correlation between the mark and the preceding and following spaces of the mark; and (e) shifting the bias power control signal, the erase power control signal, the peak power control signal and the cooling power control signal with reference to the pulse variation determined in the step (d).

[0014] In another aspect of the present invention, there is provided a recording apparatus which is adaptive to various optical recording media, the recording apparatus comprising: a microcomputer for storing timing data which represent

starting and ending positions of a first pulse, a multi-pulse train, a last pulse and a cooling pulse which constitute write pulses for each optical recording medium, the timing data obtained relative to rising and falling edges of the mark; a base signal generation unit for generating base signals which are used to generate write pulse control signals based on the timing data from the microcomputer, in synchronism with an nonreturn to zero inverted (NRZI) signal; a write waveform generation unit for generating the write pulse control signals in response to the base signals from the base signal generation unit; and a laser diode driver for driving a laser diode in response to the write pulse control signals from the write waveform generation unit.

[0015] For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings in which:

Figure 1 shows waveforms of write pulses for use in forming marks;

Figure 2 shows waveforms of other write pulses for forming a write mark;

Figure 3 shows waveforms of write pulses for each optical recording medium, corresponding to an input nonreturn to zero inverted (NRZI) signal;

Figure 4 is a schematic diagram illustrating a write pulse control signal generating method according to a preferred embodiment of the present invention;

Figure 5 shows waveforms of write pulses for each optical recording medium with respect to the settings of Table 1;

Figure 6 is a block diagram of a recording apparatus according to a preferred embodiment of the present invention;

Figure 7 is a block diagram showing the structure of the base signal generation unit of Figure 5; and

Figure 8 is a block diagram showing the structure of the write waveform generation unit of Figure 5.

[0016] Figure 1 shows waveforms of write pulses for use in forming marks, where a waveform (a) represents non return to zero inverted (NRZI) data, and a waveform (b) represents write pulses which are used in recording the data of the waveform (a) in a disk. The write pulses of the waveform (b) are the combination of a read power control signal READ POWER of a waveform (c), a peak power control signal PEAK POWER of a waveform (d), and a bias power control signal BIAS POWER of a waveform (e). A write waveform generator receives the NRZI signal of the waveform (a) to generate the control signals illustrated in the waveforms (c) through (e) of Figure 1. When the write wavefom generator provides the control signals to a laser diode driver, the laser diode driver drives a laser diode to generate the write pulses shown in the waveform (b) of Figure 1. The waveforms of Figure 1 illustrate the case where write pulses are generated using three control signals.

[0017] Figure 2 shows waveforms of another set of write pulses for use in forming marks when four control signals are used. In Figure 2, a waveform (a) represents NRZI data, and a waveform (b) represents write pulses which are used in recording the data of the waveform (a) in a disc. The write pulses of the waveform (b) are the combination of a bias power control signal BIAS POWER of a waveform (c), an erase power control signal ERASE POWER of a waveform (d), a peak power control signal PEAK POWER of a waveform (e) and a cooling power control signal COOLING POWER of a waveform (f).

[0018] The write pulses of the waveform (b) of Figure 1 conforms to a 2.6 gigabyte (Gb) DVD-RAM standard. According to a 2.6 Gb DVD-RAM standard, a write pulse consists of a first pulse, a multi-pulse train, a last pulse and a cooling pulse. Also, the number of multiple pulses varies depending on the length of the mark while a first pulse and a last pulse are always present.

[0019] The first pulse is for forming a rising edge of a mark. The multi-pulse train, which is interposed between the first pulse and the last pulse, consists of a plurality of pulses in order to lower the unevenness of marks, which occurs due to the concentration of heat, wherein the number of pulses depends on the length of the mark. The last pulse is for forming a trailing edge of a mark, and the cooling pulse, which is located at the rear of the last pulse, is for preventing the mark from becoming too long.

[0020] Optical recording media such as DVD-RAM, DVD-R, DVD-RW, DVD+RW or CD-RW have different recording characteristics. Although the mark has an equal length in each optical recording medium, shapes of write pulses differ according to the type of recording mediums or the recording speed. In particular, the starting positions and the length of the first pulse, the multi-pulse train, the last pulse and the cooling pulse are different.

[0021] For adaptively recording to optical recording media, the first pulse, the multi-pulse train, the last pulse, the cooling pulse and the like are shifted in the time domain in order to eliminate jitter from the mark. Such cases are

illustrated in the middle and right columns of the waveforms of Figure 2.

[0022] Figure 3 shows waveforms illustrating the shapes of write pulses for each optical recording medium which correspond to an input NRZI signal. In particular, a waveform (a) represents an input NRZI signal, a waveform (b) represents write pulses in a 4.7 Gb DVD-RAM, a waveform (c) represents write pulses in a DVD-R, a waveform (d) represents write pulses in a DVD-RW, a waveform (e) represents write pulses a DVD+RW, and a waveform (f) represents a quad speed CD-RW.

[0023] As shown in Figure 3, because the shapes of the write pulses differ in each optical recording medium, for adaptively recording to multiple optical recording media, a recording apparatus requires a plurality of write waveform generators suitable for each recording medium, thereby increasing the amount of hardware.

[0024] In the preferred write pulse control signal generating method, the starting position and ending position of each pulse constituting the write pulses are tabulated as timing data, and the timing data stored in the table are read in synchronism with an input NRZI signal, and write pulse control signals are generated by the read timing data.

[0025] Figures 4 and 5 are schematic diagrams illustrating a write pulse control signal generating method according to a preferred embodiment of the present invention. In Figure 4, a waveform (a) represents an input NRZI signal, a waveform (b) represents setting points based on which timing data for the starting and ending positions of a first pulse, a multi-pulse train, a last pulse and a cooling pulse are to be obtained, and a waveform (c) represents an example of a write pulse, which is generated based on the timing data, in a DVD-RAM.

[0026] In order to obtain timing data for the starting position of the first pulse, eight setting points C_SFP[2..0] before and after a rising edge of a mark are set with an equal interval. The starting position of the first pulse is designated by a 3-bit information which determines one of the eight setting points C_SFP[2..0] as the starting position of the first pulse.

[0027] In order to obtain timing data for the ending position of the first pulse, eight setting points C_EFP[2..0] before and after the rising edge of the mark are set with an equal interval. The ending position of the first pulse is designated by 3 bits of information which determines one of the eight setting points C_EFP[2..0] as the ending position of the first pulse.

[0028] Preferably, the base of the setting points C_SFP[2..0] for representing the starting position of the first pulse, and that of the setting points C_EFP[2..0] for representing the ending position of the first pulse, have a predetermined interval. Since the first pulse has a width of at least 0.5T, the base of the first point C_SFP[0] of the setting points C_SFP[2..0] for the starting position of the first pulse is separated by 0.5T from the base of the first point C_EFP[0] of the setting points C_EFP[2..0] for the ending position of the first pulse. Here, "T" represents a cycle of a reference clock for each optical recording medium.

[0029] In order to obtain timing data for the starting position of the multi-pulse train, eight setting points C_SMP[2..0] before and after the rising edge of the mark are set with an equal interval. The starting position of the multi-pulse train may be determined by one of the setting points C_SMP[2..0].

[0030] Preferably, the base of the first point of the setting points C_SFP[2..0] for the starting position of the first pulse is separated by a predetermined interval from base of the first point of the setting points C_SMP[2..0] for the starting position of the multi-pulse train. Since the starting position of the first pulse is separated by at least 1T from that of the multi-pulse train, the base of the first point C_SFP[0] of the setting points for the starting position of the first pulse is separated by 1T from the base of the setting points for the starting position of the multi-pulse train. The ending position of the multi-pulse train corresponds to the starting position of the last pulse, so that determination of the ending position of the multi-pulse train is not specified.

[0031] In order to obtain timing data for the starting position of the last pulse, eight setting points C_SLP[2..0] before and after a falling edge of the mark are set with an equal interval. The starting position of the last pulse is designated by 3 bits of information which determines one of the eight setting points C_SLP[2..0] as the starting position of the last pulse.

[0032] In order to obtain timing data for the ending position of the last pulse, eight setting points C_ELP[2..0] before and after the falling edge of the mark are set with an equal interval. The ending position of the last pulse is designated by 3 bits of information which determines one of the eight setting points C_ELP[2..0] as the ending position of the last pulse.

[0033] Preferably, the base of the setting points C_SLP[2..0] for representing the starting position of the last pulse, and that of the setting points C_ELP[2..0] for representing the ending position of the last pulse have a predetermined interval. Since the last pulse has a width of at least 0.5T, the base of the setting points C_SLP[2..0] for the starting position of the last pulse is separated by 0.5T from the base of the setting points C_ELP[2..0] for the ending position of the last pulse.

[0034] The starting position of the cooling pulse corresponds to the ending position of the last pulse, so that the starting position of the cooling pulse is not separately determined. For timing data for the ending position of the cooling pulse, eight setting points C_ELC[2..0] before and after the falling edge of the mark are set with an equal interval. The ending position of the cooling pulse is designated by one of the setting points C_ELC[2..0].

[0035] Preferably, the base of the setting points C_ELP[2..0] for representing the ending position of the last pulse,

and the base of the setting points C_ELC[2..0] for representing the ending position of the cooling pulse have a predetermined interval. Since the cooling pulse has a width of at least 1T, the base of the setting points C_ELP[2..0] for the ending position of the last pulse is separated by 1T from the base of the setting points C_ELC[2..0] for the ending position of the cooling pulse.

[0036] As illustrated in Figure 4, the timing data for the write pulses, which are adaptive to various optical recording media, is obtained based on the setting points. Table 1 shows an example of a table used to generate write pulses according to the type of optical recording medium.

Table 1

Media Type	Based Setting Point Value					
	S_SFP[2..0]	C_EFP[2..0]	C_SLP[2..0]	C_ELP[2..0]	C_SMP[2..0]	C_ELC[2..0]
4.7Gb DVD-RAM	2	3	2	3	2	4
2.6Gb DVD-RAM	3	4	2	3	3	4
DVD-R	4	6	4	3	5	2
DVD-RW	3	4	4	3	3	4
DVD+RW	2	1	2	1	1	3
CD-RW	3	4	2	2	2	2

[0037] The base of the setting points C_SFP[2..0] precedes the rising edge of the NRZI signal by 1T. The base of the setting points C_SLP[2..0] precedes the falling edge of the NRZI signal by 3T.

[0038] Figure 5 shows waveforms of write pulses at the setting point values of Table 1 according to the types of optical recording medium. In Figure 5, a waveform (a) represents write pulses for a 4.7 Gb DVD-RAM and a waveform (b) represents write pulses for a DVD-R, a waveform (c) represents write pulses for a DVD-RW, a waveform (d) represents write pulses for a DVD+RW, and a waveform (e) represents write pulses for a quad speed CD-RW. For example, the waveform (a) of Figure 5 is of a write signal at the DVD-RAM where C_SFP[2..0]=3, C_EFP[2..0] =4, C_SMP[2..0] =3, C_SLP[2..0]=2, C_ELP[2..0]=3 and C_ELC[2..0] =4.

[0039] Figure 6 is a block diagram of a recording apparatus according to a preferred embodiment of the present invention. The recording apparatus of Figure 6 is for adaptively recording to each optical recording medium, in which the position of write pulses is shifted based on correlation between the current mark and the preceding and following spaces of the current mark. The recording apparatus includes a data determinator 100, a write waveform generation unit 120, a laser diode (LD) driver 140, an LD 160, an automatic laser-diode power control (ALPC) circuit 200, a driver microcomputer 102, a shift table storage unit 104 for storing a table of variations of write pulses in a time domain, and a base signal generation unit 106.

[0040] The ALPC circuit 200, which includes a photo diode (PD) 202, a variable gain amplifier (VGA) 204, a comparator (COMP) 206, an up/down counter 208, and a digital-to-analog converter (DAC) 210, performs ADPC operation to maintain the level of an optical signal that is output from the LD 160.

[0041] The level of write pulses from the LD 160 is controlled by optical output control data provided by the up/down counter 208 of the ALPC circuit 200. The PD, a light receiving device, receives the optical signal reflected by the disc 180, and the VGA 204 amplifies the optical signal received by the PD 202. Also, the COMP 206 compares the voltage level output from the VGA 240 and a reference voltage Vref provided by the driver microcomputer 102. Here, the level of reference voltage Vref is determined according to the power of write pulses required in a normal record mode. The up/down counter 208 performs downcounting if the COMP 206 determines that the level of the optical signal is higher than the reference voltage Vref. Otherwise, the up/down counter 208 performs upcounting. The count result of the up/down counter 208 is provided as the optical output control data to the LD driver 140 through the DAC 210. During normal record mode, the optical output control data from the up/down counter 208 is provided to the DAC 210.

[0042] The recording apparatus of Figure 6 operates both in a normal record mode and an adaptive record mode. In the normal record mode, write pulse control signals are generated according to signals (hereinafter, referred to as base signals) generated by the base signal generation unit 106. The base signal includes a first pulse start signal S_SFP, a first pulse end signal S_EFP, a multi-pulse train start signal S_SMP, a fixed width multi-pulse train signal MP, a variable-width multi-pulse train start signal MP_S, a variable-width multi-pulse train end signal MP_E, a last pulse start signal S_SLP, a last pulse end signal S_ELP and a cooling pulse end signal S_ELC.

[0043] Also, in the adaptive record mode, the write pulse control signals are shifted based on the time domain shift information stored in the shift table storage unit 104, in response to the base signals generated in the base signal generation unit 106.

[0044] In the recording apparatus of Figure 6, the shift table storage unit 104, which stores a table of variations of write pulses in a time domain according to correlation between a mark and the preceding and following spaces of the mark, is initialized in synchronism with the initiation of the driver microcomputer 102. During the initiation of the shift table storage unit 104, the driver microcomputer 102 reads a shift table recorded in a lead-in/out area, and stores the shift table in the shift table storage unit 104. The variations of write pulses in the time domain according to the correlation between a mark and the preceding and following spaces of the mark, which are tabulated in the shift table, are essential for optimal recording.

[0045] In the adaptive recording according to the type of optical recording medium, the write waveform generation unit 120 shifts the write pulses generated by the LD 160 in the time domain based on the variations of write pulses in the time domain which is served by the shift table storage unit 104. The variations of write pulses in the time domain according to the correlation between a mark and the preceding and following spaces of the mark may differ depending on the type of the disc 180, and are usually investigated and recorded in the lead-in/out area of the disc 180 by a manufacturer.

[0046] The data determinator 100 receives NRZI data and determines the correlation between a mark and the preceding and following spaces of the mark, and provides the shift table storage unit 104 with the determination result. The shift table storage unit 104 provides the variations of write pulses in the time domain based on the determination result from the data determinator 100 to the write waveform generation unit 120. The write waveform generation unit 120 generates write pulse control signals with reference to the variations of write pulses in the time domain, which are provided by the shift table storage unit 104, in response to the base signal from the base signal generation unit 106. The write pulses generated by the write waveform generation unit 120 are provided to the LD driver 140.

[0047] The LD driver 140 drives the LD 160 in response to the signals from the write waveform generation unit 120, for example, a record power control signal, an erase power control signal, a bias power control signal and a cooling power control signal, such that write pulses are generated.

[0048] For example, when the NRZI data of the waveform (a) of Figure 2 is input to the data determiner 100, the write waveform generation unit 120 generates the control signals BIAS POWER (waveform (c) of Figure 2), ERASE POSER (waveform (d) of Figure 2), PEAK POWER (waveform (e) of Figure 2) and COOLING POWER (waveform (f) of Figure 2). Then, the LD driver 140 controls the LD 160 in response to the write pulse control signals applied from the write waveform generation unit 120 such that the write pulses having the waveform (b) of Figure 2 are generated.

[0049] The LD driver 140 controls the output level of the LD 160 in accordance with the write pulse control signals, and the optical output control data from the DAC 210. The write pulses generated by the LD 160 are irradiated onto the disc 180 such that data are recorded thereon. The position of the write pulses generated by the LD 160 are adaptively varied as shown in the middle and right columns (Examples 1 and 2) of Figure 2, according to the correlation between the mark and the preceding and following spaces of the mark.

[0050] Figure 7 is a block diagram showing a detailed structure of the base signal generation unit 106 of Figure 6. The base signal generation unit includes a first shift register 700, a base signal generator 702, a second shift register 704, a third shift register 706, a plurality of multiplexers (MUXs) 708 through 718, a latch 720 and a gate 722. The first shift register 700 shifts an input NRZI signal and applies the shifted signal to the base signal generator 702. The base signal generator 702 generates the base signal based on the shifted NRZI signal. This base signal includes a first base pulse which is generated 1T in advance of the rising edge of a mark of the NRZI signal from the first shift register 700, and a second base pulse which is generated 3T in advance of the falling edge of the mark. The first base pulse represents the base point (first base point) of the setting points C_SFP[2..0] for the starting position of the first pulse, and the second base signal represents the base point (second base point) of the setting points C_SLP[2..0] for the starting position of the last pulse (see Figure 4).

[0051] The second shift register 704 outputs 10 pulse signals (first setting signals) with an interval of 0.5T therebetween, wherein the last pulse signal is shifted by 5T. The first through eighth pulse signals of the 10 pulse signals from the second shift register 704, which correspond to the setting points C_SFP[2..0] for the starting position of the first pulse (see Figure 4), are input to the first MUX 708. The first MUX 708 selectively outputs one of the eight pulse signals to the write waveform generation unit 120, via the latch 720, depending on the type of optical recording medium used. The output of the first MUX 708 is a first pulse start signal S_SFP that indicates the starting position of the first pulse.

[0052] The second through ninth pulse signals of the 10 pulse signals from the second shift register 704, which correspond to the setting points C_EFP[2..0] for the ending position of the first pulse (see Figure 4), are input to the second MUX 710. The second MUX 710 selectively outputs one of the eight pulse signals to the write waveform generation unit 120, via the latch 720, depending on the type of optical recording medium used. The output of the second MUX 710 is a first pulse end signal S_EFP that indicates the ending position of the first pulse. The third through tenth pulse signals of the 10 pulse signals from the second shift register 704, which correspond to the setting points C_SMP [2..0] for the starting position of the multi-pulse train (see Figure 4), are input to the third MUX 712. The third MUX 712 selectively outputs one of the eight pulse signals to the write waveform generation unit 120, via the latch 720, depending on the type of optical recording medium used. The output of the third MUX 712 is a multi-pulse train start signal S_SMP

that indicates the starting position of the multi-pulse train.

[0053] Also, the third shift register 706 outputs 10 pulse signals (second setting signals) with an interval of 0.5T therebetween, wherein the last one of the 10 pulse signals are shifted by 5T. The first through eighth pulse signals of the 10 pulse signals from the third shift register 706, which correspond to the setting points C_SLP[2..0] for the starting position of the last pulse (see Figure 4), are input to the fourth MUX 714. The fourth MUX 714 selectively outputs one of the eight pulse signals to the write waveform generation unit 120, via the latch 720, depending on the type of optical recording medium used. The output of the fourth MUX 714 is a last pulse start signal S_SLP that indicates the starting position of the last pulse.

[0054] The second through ninth pulse signals of the 10 pulse signals from the third shift register 706, which correspond to the setting points C_ELP[2..0] for the ending position of the last pulse (see Figure 4), are input to the fifth MUX 716. The fifth MUX 716 selectively outputs one of the eight pulse signals to the write waveform generation unit 120, via the latch 720, depending on the type of optical recording medium used. The output of the fifth MUX 716 is a last pulse end signal S_ELP that indicates the ending position of the last pulse. The third through tenth pulse signals of the 10 pulse signals from the second shift register 704, which correspond to the setting points C_ELC[2..0] for the ending position of the cooling pulse (see Figure 4), are input to the sixth MUX 718. The sixth MUX 718 selectively outputs one of the eight pulse signals to the write waveform generation unit 120, via the latch 720, depending on the type of optical recording medium used. The output of the sixth MUX 718 is a cooling pulse end signal S_ELC that indicates the ending position of the cooling pulse.

[0055] Selection signals for selecting the first through sixth MUXs 708 through 718 are looked up in a shift table storage unit storing Table 1. The driver microcomputer 102 reads the based setting point values C_SFP[2..0], C_EFP [2..0], C_SMP[2..0], C_SLP[2..0], C_ELP[2..0] and C_ELC[2..0] from the table depending on which optical recording medium is being used, and outputs selection signals for the first through sixth MUXs 708 through 718.

[0056] The gate 722 generates signals for generating the multi-pulse train. In particular, the gate 722 essentially generates a fixed-width multi-pulse train signal MP, which is obtained by AND-gating the NRZI signal from the first shift register 700 with a system clock signal. Also, the gate 722 is a variable-width multi-pulse start signal MP_S, which is synchronized with the fixed-width multi-pulse train signal MP, and a variable-width multi-pulse train end signal MP_E delayed slightly with respect to the variable-width multi-pulse train start signal MP_S.

[0057] The latch 720 receives the first pulse start signal S_SFP from the first MUX 708, the first pulse end signal S_EFP from the second MUX 710, the multi-pulse start signal S_SMP from the third MUX 712, the last pulse start signal S_SLP from the fourth MUX 714, the last pulse end signal S_ELP from the fifth MUX 716, the cooling pulse end signal S_ELC from the sixth MUX 718 and the fixed-width multi-pulse signal MP from the gate 722, latches the input signals such that they are synchronized with the system clock, and outputs the resultant signals. The reason for the latching is that these signals may be asynchronized because they are processed through different paths.

[0058] Figure 8 is a block diagram showing the structure of a write waveform generation unit 120 of Figure 6. The write waveform generation unit includes a peak power control signal generation portion 800, a cooling power control signal generator 810, an erase power control signal generator 820, and a multi-pulse train generator 830.

[0059] In particular, the peak power control signal generation portion 800, which includes a first pulse generator 802, a last pulse generator 804 and a gate 806, receives the first pulse start signal S_SFP, the first pulse end signal S_EFP, the last pulse start signal S_SLP, the last pulse end signal S_ELP and the bias power control signal BIAS POWER, to generate the peak power control signal PEAK POWER shown as the waveform (e) of Figure 2. In particular, the first pulse generator 802 receives the first pulse start signal S_SFP and the first pulse end signal S_EFP from the base signal generation unit 106, to generate a first pulse. The last pulse generator 804 receives the last pulse start signal S_SLP and the last pulse end signal S_ELP from the base signal generation unit 106, to generate a last pulse. The gate 806 performs an OR operation on the first pulse from the first signal generator 802, the last pulse from the last pulse generator 804, and the bias power control signal BIAS POWER from the multi-pulse train generator 830, resulting in the peak power control signal PEAK POWER shown in the waveform (e) of Figure 2.

[0060] The cooling power control signal generator 810 receives the cooling pulse end signal S_ELC from the base signal generation unit 106 and the last pulse from the last pulse generator 804 to generate the cooling power control signal COOLING POWER shown in the waveform (f) of Figure 2. The erase power control signal generator 820 receives the first pulse start signal S_SFP and the cooling pulse end signal S_ELC to generate the erase power control signal ERASE POWER shown in the waveform (d) of Figure 2. The multi-pulse train generator 830 receives the fixed-width multi-pulse signal MP, the variable-width multi-pulse start signal MP_S and the variable-width multi-pulse end signal MP_E, which are provided by the base signal generation unit 106, to generate the bias power control signal BIAS POWER shown in the waveform (c) of Figure 2.

[0061] In particular, the first pulse generator 802 of the peak power control signal generation portion 800 includes a first delay 802a, a second delay 802b, multiplexers 802c and 802d, and a first latch 802e. The first delay 802a delays the first pulse start signal S_SFP from the base signal generation unit 106 by a period of time set by a signal TB1ST [5..0] from the shift table storage unit 104. By the operation of the first delay 802a, the rising edge of the first pulse can

be shifted.

[0062] The second delay 802b delays the first pulse end signal S_EFP from the base signal generation unit 106 by a period of time set by a signal T_FP[7..0] or T_EFP from the shift table storage unit 104. By the operation of the second delay 802b, the falling edge of the first pulse can be shifted. Selection of the signal T_FP[7..0] or T_EFP[5..0] is controlled by a signal CASE2. The signal CASE2 determines a write pulse shift mode. The write pulse shift mode includes a variable-width mode Casel for varying the width of the write pulse, and a position shift mode Case2 for shifting the position of the write pulse.

[0063] The outputs from the first and second delays 802a and 802b are applied as clock and reset signals, respectively, for the first latch 802e. The first latch 802e is enabled by a write mode control signal WMODE, is set by the output from the first delay 802a, and is reset by the output from the second delay 802b. The first pulse, which has a rising edge set by the first pulse start signal S_SFP and a falling edge set by the first pulse end signal S_EFP, is obtained by the operation of the first latch 802e. In the adaptive record mode, the width of the first pulse is determined by the signal T_FP[7..0] or T_EFP[5..0].

[0064] The last pulse generator 804 includes a third delay 804a, a fourth delay 804b, multiplexers 804c, 804d and 804e and a second latch 804f. The third delay 804a delays the last pulse start signal S_SLP from the base signal generation unit 106 by a period of time set by a signal T_SLP[7..0] or TBLST[5..0] from the shift table storage unit 104. By the operation of the third delay 804a, the rising edge of the last pulse can be shifted. Selection of the signals T_SLP [7..0] or TBLST[5..0] is controlled by the signal CASE2. The fourth delay 804b delays the last pulse end signal S_ELP from the base signal generation unit 106 by a period of time set by a signal T_LP[7..0] or TBLST[5..0] from the shift table storage unit 104. By the operation of the fourth delay 804b, the falling edge of the last pulse can be shifted. Selection of the signal T_LP or T_ELP[5..0] is controlled by the signal CASE2.

[0065] The outputs of the third and fourth delays 804a and 804b are applied as clock and reset signals, respectively, for the second latch 804f. The second latch 804f is enabled by the write mode control signal WMODE, is set by the output from the third delay 804a, and is reset by the output from the fourth delay 804b. The last pulse, which has a rising edge set by the last pulse start signal S_SLP and a falling edge set by the last pulse end signal S_ELP, is obtained by the operation of the second latch 804f. In the adaptive record mode, the width of the last pulse is determined by the signal T_SLP[7..0], T_LP[7..0] or TBLST[5..0].

[0066] The gate 806 of the power peak control signal generation portion 800 performs an OR-operation on the first pulse from the first signal generator 802, the last pulse from the last pulse generator 804 and the bias control signal from the multi-pulse train generator 830, and outputs the operation result.

[0067] The cooling power control signal generator 810 of the write waveform generation unit 120 includes a fifth delay 810a, multiplexers 810b and 810c, a third latch 810d and inverters 810e and 810f. The fifth delay 810a delays the cooling pulse end signal S_ELC from the base signal generation unit 106 by a period of time set by a signal TBLC [5..0] or T_LC[7..0] from the shift table storage unit 104. Selection of the signal TBLC[5..0] or T_LC[7..0] is controlled by a signal Adap_LC. By the operation of the fifth delay 810a, the falling edge of the cooling pulse can be controlled. The rising edge of the cooling pulse is set by the output from the last pulse generator 804 or the cooling pulse end signal S_ELC. The multiplexer 810b selects the output from the last pulse generator 804 or the cooling pulse end signal S_ELC in response to a signal LC_sel.

[0068] The outputs of the multiplexer 810b and the fifth delay 810a are applied as clock and reset signals, respectively, for the third latch 810d. The third latch 810d is enabled by the write mode control signal WMODE, is set by the output from the multiplexer 810b, and is reset by the output from the fifth delay 810d. The cooling power control signal, which has a rising edge set by the cooling pulse end signal S_ELC and a falling edge set by the last pulse end signal S_ELP from the last pulse generator 804, is obtained by the operation of the second latch 804f. In the adaptive record mode, the width of the cooling power control signal is determined by the signal TBLC[5..0] or T_LC[7..0].

[0069] The erase power control signal generator 820 of the write waveform generation unit 120 includes an OR gate 820a, an inverter 820b and a fourth latch 820c. The OR gate 820a performs an OR-operation on the output from the fifth delay 810a and a signal start_B1, and outputs the operation result. The inverter 820b inverts the output from the first delay 802a of the first pulse generator 802, and outputs the inverted result. The fourth latch 820c is enabled by the write mode control signal WMODE, is set by the output from the OR gate 810a, and is reset by the output from the inverter 820b. The erase power signal, which has a rising edge set by the output from the OR gate 820a and a falling edge set by the is set by the output from the inverter 820b, can be obtained by the operation of the fourth latch 820c.

[0070] The multi-pulse train generator 830 of the write waveform generation unit 120 includes a sixth delay 830a, an AND gate 830b, a fifth latch 830c and a multiplexer 830d. The sixth delay 830a delays the variable-width multi-pulse train end signal MP_E from the base signal generation unit 106 by a period of time set by a signal T_MP from the shift table storage unit 104. By the operation of the sixth delay 830a, the width of the multi-pulse train can be varied. The AND gate 830b performs an AND-operation on the output from the sixth delay 830a and a signal var_MP, and outputs the operation result. The signal var_MP is for enabling or disabling the variation of the multi-pulse train.

[0071] The variable-width multi-pulse start signal MP_S from the base signal generation unit 106, and the output

from the AND gate 830b are applied as clock and reset signals, respectively, for the fifth latch 830c. The fifth latch 830c is enabled by the write mode control signal WMODE, is set by the variable-width multi-pulse start signal MP_S, and is reset by the output from the AND gate 830b. The multi-pulse train that has a variable width can be obtained by the operation of the fifth latch 830c. The multiplexer 830d selectively outputs the output from the fifth latch 830c or the fixed-width multi-pulse signal MP from the base signal generation unit 106, in response to the signal var_MP.

[0072] The write waveform generation unit shown in Figure 8 can be applied to generate write pulses for two channels. For generation of write pulses for two channels, which have only bias and peak levels, the erase power control signal ERASE POWER shown in the waveform (g) of Figure 2 is used instead of that shown in the waveform (d) of Figure 2.

[0073] As described above, the recording apparatus according to the present invention can store write pulses, which are adaptive to various optical recording media, in the form of timing data, and generate base signals based on the timing data. Also, the write pulse control signals can be generated by the base signals, which controls timing of the write pulses such that the optical recording can be realized adaptively to various optical recording media.

[0074] While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention as defined by the appended claims.

[0075] The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

[0076] All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

[0077] Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

[0078] The invention is not restricted to the details of the foregoing embodiment(s). The invention extend to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

Claims

1. A method for generating write pulse control signals which are adaptive to various optical recording media, the method comprising the steps of:

   (a) obtaining timing data with respect to starting and/or ending positions of pulses, relative to rising and falling edges of a mark, wherein the timing data comprises a first pulse, a multi-pulse train, a last pulse and a cooling pulse, and the starting and ending positions of the pulses are varied for various optical recording media;

   (b) storing the timing data from the step (a); and

   (c) generating a bias power control signal, an erase power control signal, a peak power control signal and a cooling power control signal in synchronism with an input nonreturn to zero inverted (NRZI) signal, based on the timing data for each optical recording medium.

2. The method of claim 1, wherein the timing data obtained in the step (a) are for the starting and ending positions of the first pulse, the starting position of the multi-pulse train, the starting and ending positions of the last pulse, and the ending position of the cooling pulse are made into the timing data.

3. The method of claim 2, wherein a first base point for the timing data which represent the starting and ending positions of the first pulse and the starting position of the multi-pulse train is a rising edge of the mark, and a second base point for the timing data which represent the starting and ending position of the last pulse and the ending position of the cooling pulse is a falling edge of the mark.

4. The method of claim 2 or 3, wherein the first base point for the timing data which represent the starting and ending positions of the last pulse and the starting position of the multi-pulse train precedes the rising edge of the mark by 1T, and the second base point for the timing data which represent the starting and ending position of the last pulse

and the ending position of the cooling pulse precedes the falling edge of the mark by 3T, where "T" is a cycle of a reference clock for each optical recording medium.

5. The method of claim 4, wherein the starting and ending positions of the first pulse and the starting position of the multi-pulse train are set to be one of a plurality of setting points for each position, the setting points being spaced apart by an equal interval from the first base point, and the starting and ending positions of the last pulse and the ending position of the cooling pulse are set to be one of a plurality of setting points for each position, the setting points being spaced apart by an equal interval from the second base point.

6. The method of any of claims 1 to 5, wherein the step (c) comprises the sub-steps of:

(c1) generating base signals including a first pulse start signal, a first pulse end signal, a multi-pulse start signal, an erase power control signal, a last pulse start signal, a last pulse end signal and a cooling pulse end signal, which are based on the timing data for each optical recording medium; and

(c2) generating a bias power control signal, an erase power control signal, a peak power control signal and a cooling power control signal in response to the base signals.

7. The method of claim 6, further comprising the steps of:

(d) determining variations of the pulses in a time domain according to a correlation between the mark and the preceding and following spaces of the mark; and

(e) shifting the bias power control signal, the erase power control signal, the peak power control signal and the cooling power control signal with reference to the pulse variation determined in the step (d).

8. A recording apparatus which is adaptive to various optical recording media, the recording apparatus comprising:

a microcomputer (102) for storing timing data which represent starting and ending positions of a first pulse, a multi-pulse train, a last pulse and a cooling pulse which constitute write pulses for each optical recording medium, the timing data obtained relative to rising and falling edges of the mark;

a base signal generation unit (106) for generating base signals which are used to generate write pulse control signals based on the timing data from the microcomputer (102), in synchronism with an nonreturn to zero inverted (NRZI) signal;

a write waveform generation unit (120) for generating the write pulse control signals in response to the base signals from the base signal generation unit (106); and

a laser diode driver (140) for driving a laser diode in response to the write pulse control signals from the write waveform generation unit (120).

9. The recording apparatus of claim 8, wherein the microcomputer (102) stores the timing data for the starting and ending positions of the first pulse, the starting position of the multi-pulse train, the starting and ending positions of the last pulse, and the ending position of the cooling pulse.

10. The recording apparatus of claim 9, wherein a first base point for the timing data which represent the starting and ending positions of the first pulse and the starting position of the multi-pulse train is a rising edge of the mark, and a second base point for the timing data which represent the starting and ending position of the last pulse and the ending position of the cooling pulse is a falling edge of the mark.

11. The recording apparatus of claim 10, wherein the first base point for the timing data which represent the starting and ending positions of the last pulse and the starting position of the multi-pulse train precedes the rising edge of the mark by 1T, and the second base point for the timing data which represent the starting and ending position of the last pulse and the ending position of the cooling pulse precedes the falling edge of the mark by 3T, where "T" is a cycle of a reference clock for each optical recording medium.

12. The recording apparatus of claim 11, wherein the starting and ending positions of the first pulse and the starting

position of the multi-pulse train are set to be one of a plurality of setting points for each position, the setting points being spaced apart by an equal interval from the first base point, and the starting and ending positions of the last pulse and the ending position of the cooling pulse are set to be one of a plurality of setting points for each position, the setting points being spaced apart by an equal interval from the second base point.

13. The recording apparatus of any of claims 8 to 12, wherein the base signal generation unit comprises:

a base signal generator (702) for generating a first base signal indicating a first base point and a second base signal indicating a second base point, in synchronism with the NRZI signal;

a second shift register (704) for shifting the first base signal to generate first setting signals;

first, second and third multiplexers (708,710,712) for receiving the first setting signals from the second shift register (704) and the timing data from the microcomputer (102) to generate a first pulse start signal, a first pulse end signal and a multi-pulse train start signal;

a third shift register (706) for shifting the second base signal to generate second setting signals;

fourth, fifth and sixth multiplexers (714,716,718) for receiving the second setting signals from the third shift register (706) and the timing data from the microcomputer (102) to generate a last pulse start signal, a last pulse end signal and a cooling pulse end signal; and

a gate (722) for performing AND-operation on the NRZI signal and a clock signal to generate a fixed-width multi-pulse signal.

14. The recording apparatus of claim 13, wherein

the first multiplexer (708) outputs the first pulse start signal by selecting one of the first setting signals from the second shift register (704) according to the timing data indicating the starting position of the first pulse, the timing data being output from the microcomputer (102),

the second multiplexer (710) outputs the first pulse end signal by selecting one of the first setting signals from the second shift register (704) according to the timing data indicating the ending position of the first pulse, the timing data being output from the microcomputer (102),

the third multiplexer (712) outputs the multi-pulse train start signal by selecting one of the first setting signals from the second shift register (704) according to the timing data indicating the starting position of the multi-pulse train, the timing data being output from the microcomputer (102),

the fourth multiplexer (714) outputs the last pulse start signal by selecting one of the second setting signals from the third shift register (706) according to the timing data indicating the starting position of the last pulse, the timing data being output from the microcomputer (102),

the fifth multiplexer (716) outputs the last pulse end signal by selecting one of the second setting signals from the third shift register (706) according to the timing data indicating the ending position of the last pulse, the timing data being output from the microcomputer (102), and

the sixth multiplexer (718) outputs the cooling pulse end signal by selecting one of the second setting signals from the third shift register (706) according to the timing data indicating the ending position of the cooling pulse, the timing data being output from the microcomputer (102).

15. The recording apparatus of claim 14, further comprising a latch (720) for latching the outputs from the first through sixth multiplexers (708-718) to be synchronized with the clock signal and outputting the resultant signals.

16. The recording apparatus of claim 15, wherein the gate (722) generates a variable-width multi-pulse start signal (MP_S) which is synchronized with the fixed-width multi-pulse signal, and a variable-width multi-pulse end signal (MP_E)which is delayed by a predetermined period of time relative to the variable-width multi-pulse start signal.

17. The recording apparatus of claim 16, wherein the write waveform generation unit (120) comprises:

a peak power control signal generation portion (800) for receiving the first pulse start signal, the first pulse end signal, the multi-pulse train start signal, the last pulse start signal and the last pulse end signal from the base signal generation unit (106), to generate a peak power control signal;

a cooling power control signal generator (810) for receiving the last pulse end signal and the cooling pulse end signal from the base signal generation unit (106), to generate a cooling power control signal;

an erase power control signal generator (820) for receiving the first pulse start signal and the cooling pulse end signal from the base signal generation unit (106), to generate an erase power control signal; and

a multi-pulse train generator (830) for receiving the fixed-width multi-pulse signal, the variable-width multi-pulse start signal, and the variable-width multi-pulse end signal from the base signal generation unit (106) to generate a bias power control signal.

18. The recording apparatus of claim 17, wherein the peak power control signal generation portion (800) comprises:

a first pulse generator (802) for receiving the first pulse start signal and the first pulse end signal to generate a first pulse;

a last pulse generator (804) for receiving the last pulse start signal and the last pulse end signal to generate a last pulse; and

a gate (806) for performing an OR-operation on the first pulse signal, the last pulse signal and the bias power control signal which is output from the multi-pulse train generator.

19. The recording apparatus of claim 18, wherein the first pulse generator (802) comprises a first latch (802e) for generating the first pulse from when the first pulse start signal is generated until when the first pulse end signal is generated, and the last pulse generator comprises a second latch (804f) for generating the last pulse from when the last pulse start signal is generated until when the last pulse end signal is generated.

20. The recording apparatus of claim 19, wherein the recording apparatus further comprises a shift table storage unit (104) for storing a table associated with shift value of a mark in a time domain, based on correlation of the mark of the NRZI signal and the preceding and following spaces of the mark, and wherein the first pulse generator comprises first and second delays (802a,802b) for delaying the first pulse start signal and the first pulse end signal, respectively, based on a shift value from the shift table storage unit (104), and the last pulse generator comprises third and fourth delays (804a,804b) for delaying the last pulse start signal and the last pulse end signal, respectively, based on a shift value from the shift table storage unit (104).

21. The recording apparatus of claim 17, wherein the cooling power control signal generator (810) comprises a third latch (810d) for generating the cooling power control signal which is started by the cooling pulse end signal from the base signal generation unit and is ended by the last pulse end signal from the last pulse generator.

22. The recording apparatus of claim 20 or 21, further comprising a fifth delay (810a) for delaying the cooling pulse end signal based on a shift value from the shift table storage unit.

23. The recording apparatus of claim 22, wherein the erase power control signal generator (820) comprises a fourth latch for generating the erase power control signal from the generation of the output from the first delay (802a) to the generation of the output of the fifth delay (810a).

24. The recording apparatus of any of claims 17 to 23, wherein the multi-pulse train generator (830) comprises:

a fifth latch (830c) for generating a variable-width multi-pulse signal from when the variable-width multi-pulse start signal is generated until when the variable-width multi-pulse end signal is generated, the variable width multi-pulse start signal and the variable-width multi-pulse end signal being received from the base signal generation unit (106); and

a multiplexer (830d) for selectively outputting the variable-width multi-pulse signal from the fifth latch (830c) or the fixed-width multi-pulse signal from the base signal generation unit (106).

25. The recording apparatus of any of claims 20 to 24, wherein the multi-pulse train generator (830) comprises a sixth delay (830a) for delaying the variable-width multi-pulse end signal based on a shift value from the shift table storage unit (104).

FIG. 1

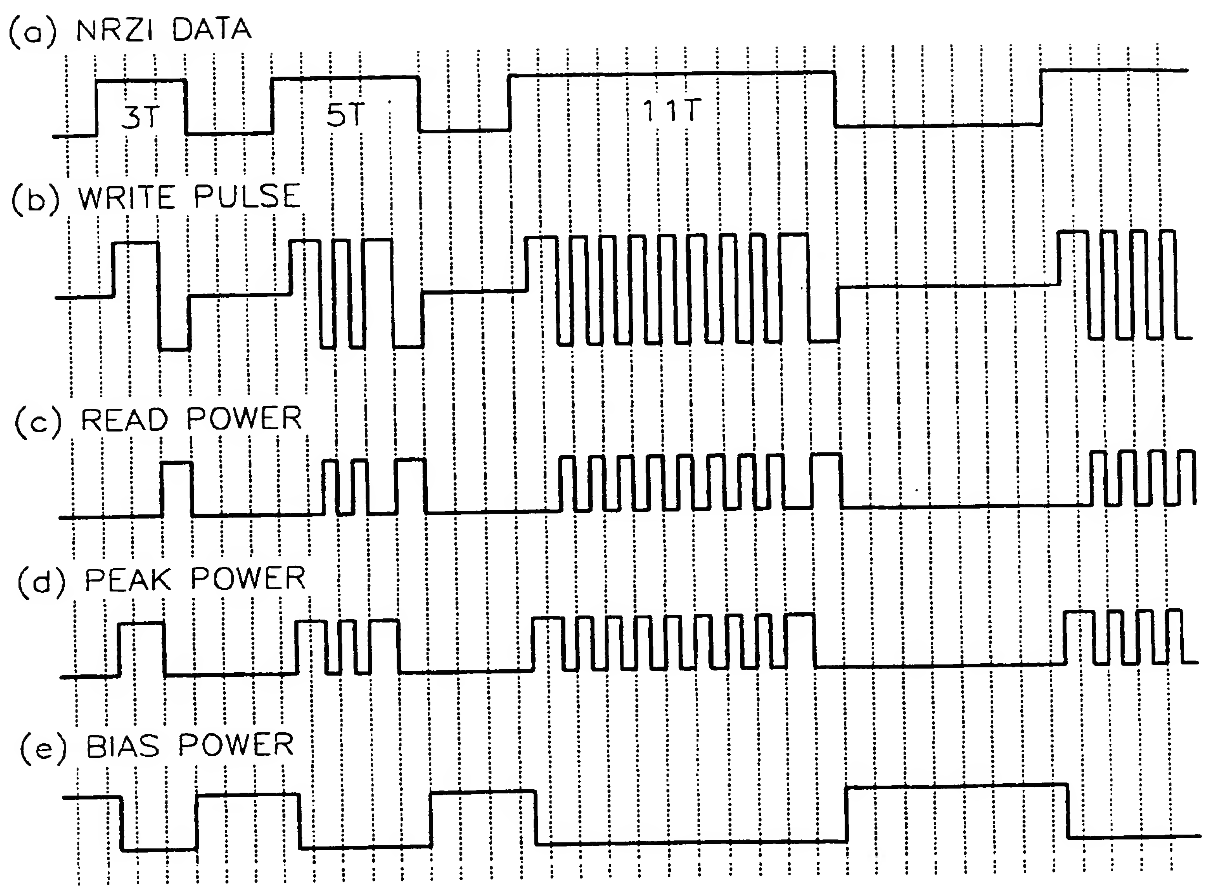

(a) NRZI DATA
3T
5T
11T
(b) WRITE PULSE
(c) READ POWER
(d) PEAK POWER
(e) BIAS POWER

FIG. 2

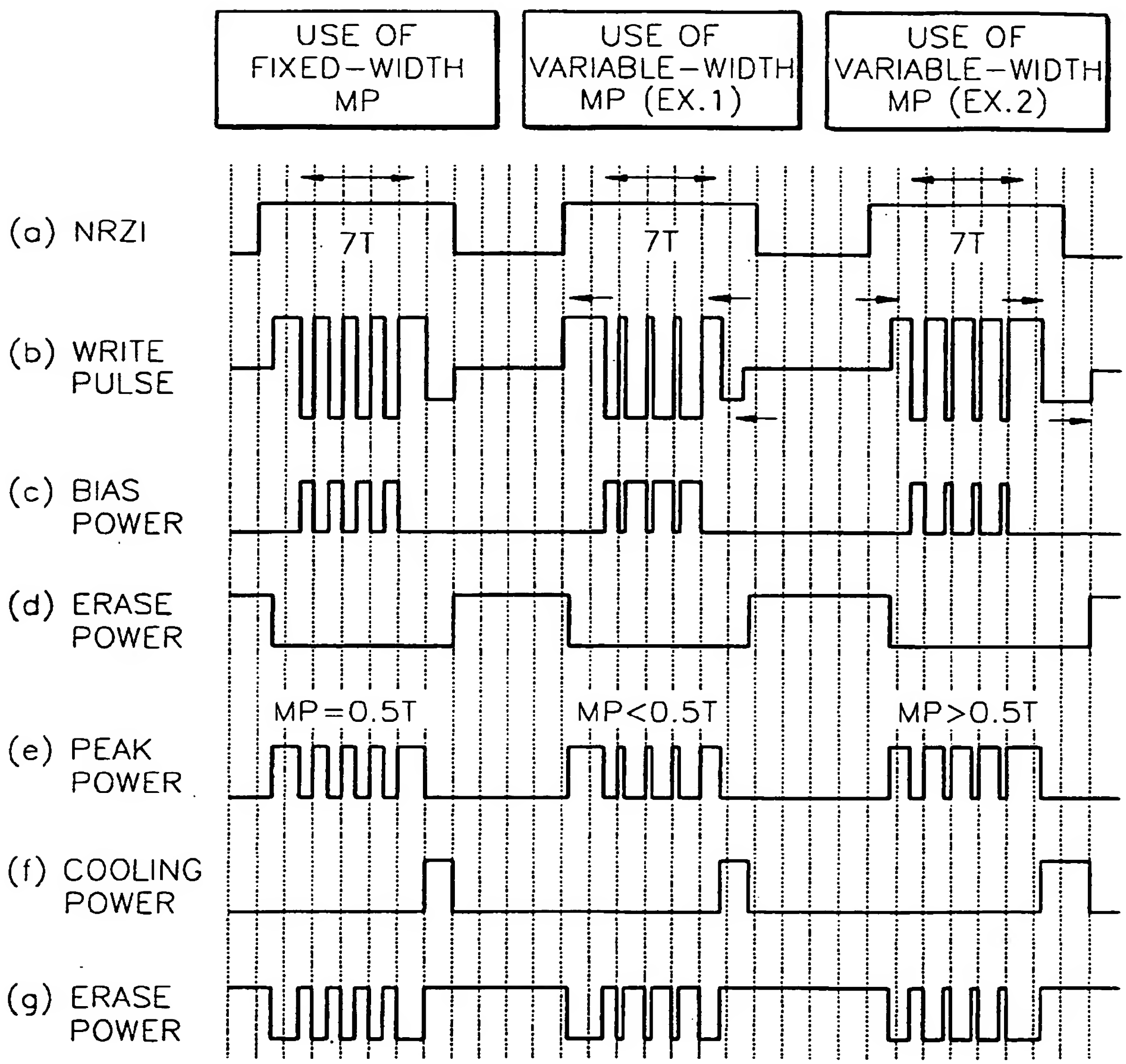
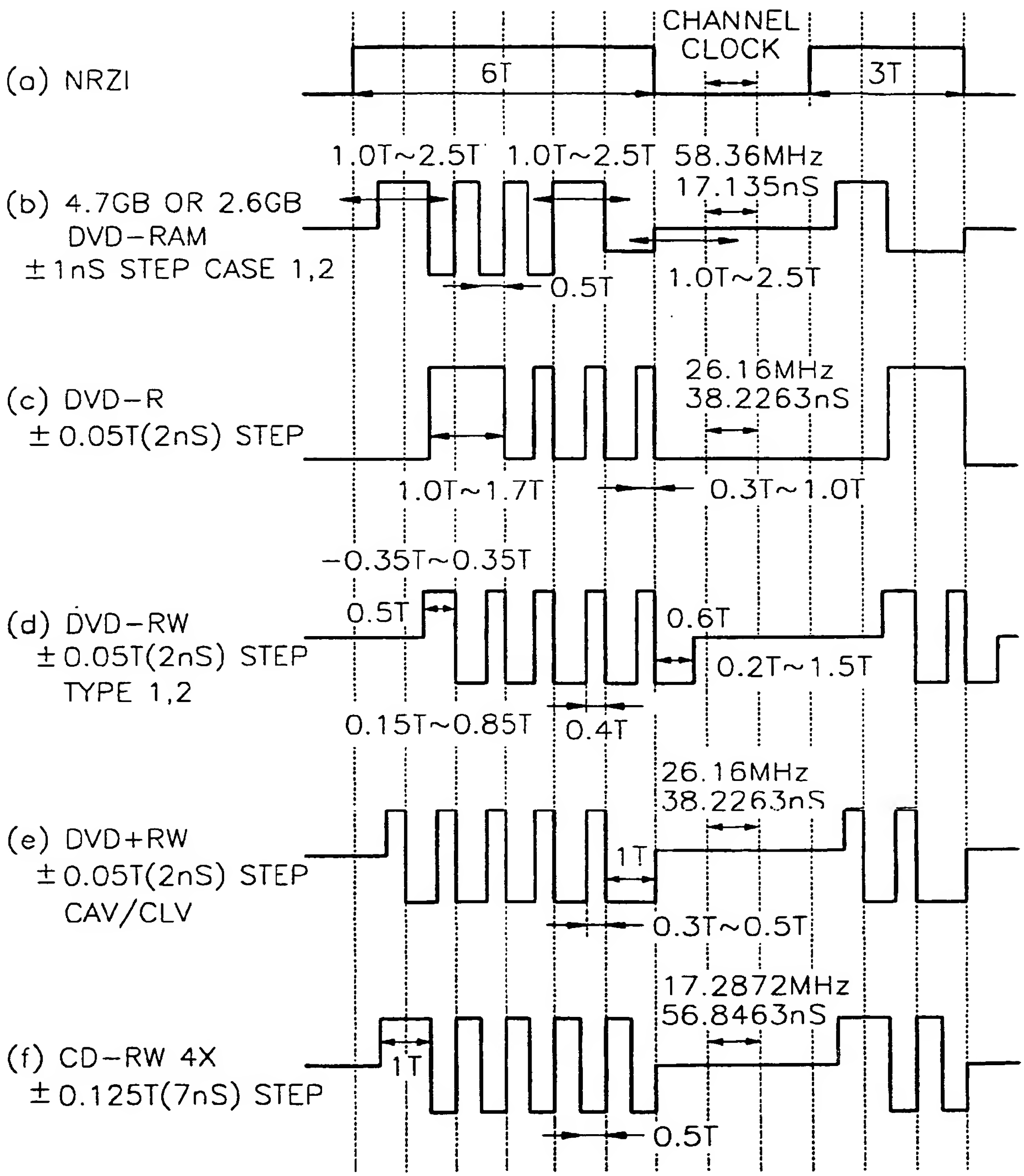
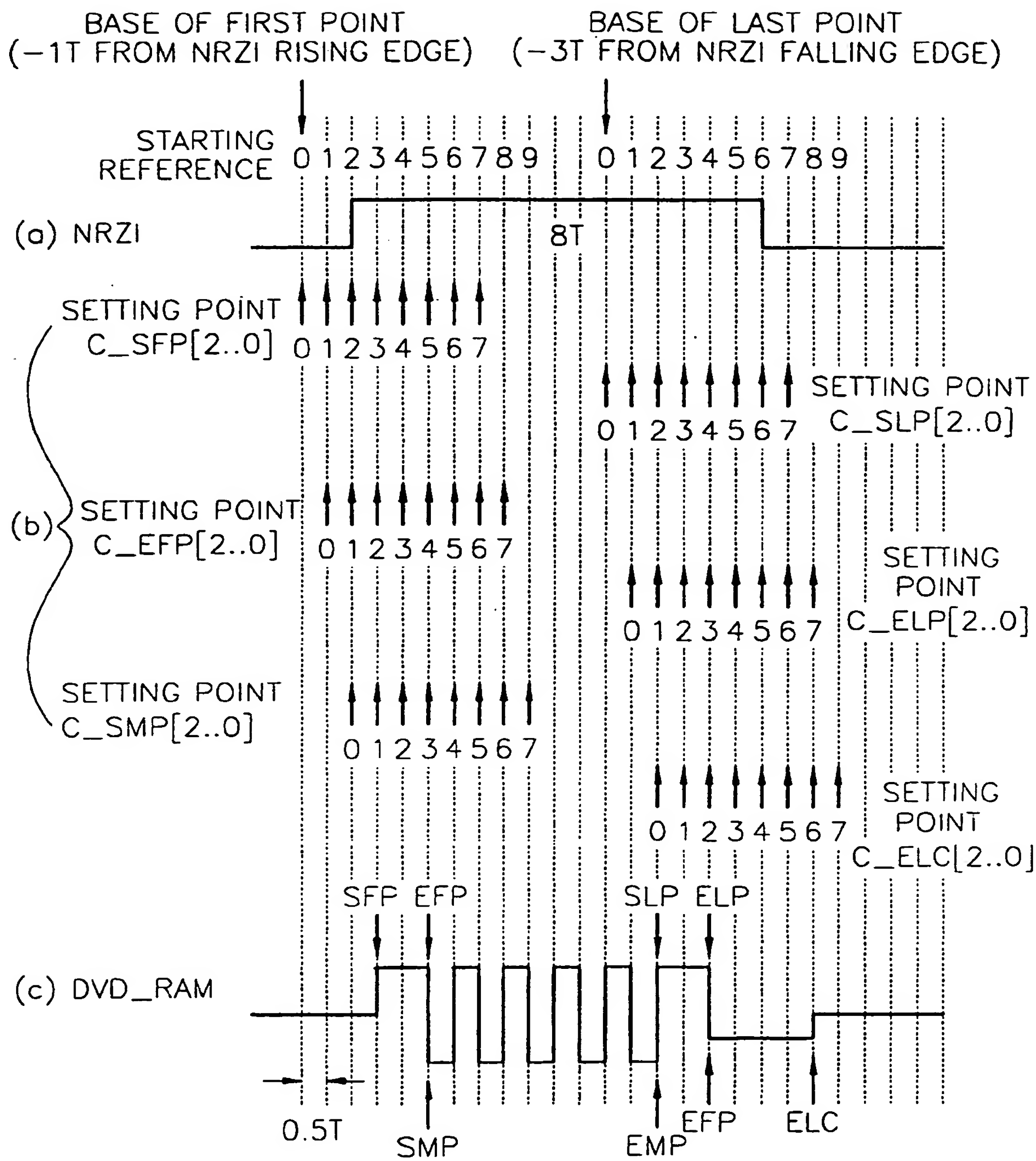

USE OF FIXED-WIDTH MP
USE OF VARIABLE-WIDTH MP (EX.1)
USE OF VARIABLE-WIDTH MP (EX.2)
(a) NRZI
7T
7T
7T
(b) WRITE PULSE
(c) BIAS POWER
(d) ERASE POWER
MP=0.5T
MP<0.5T
MP>0.5T
(e) PEAK POWER
(f) COOLING POWER
(g) ERASE POWER

FIG. 3



(a) NRZI
6T
CHANNEL
CLOCK
3T
(b) 4.7GB OR 2.6GB
DVD-RAM
±1nS STEP CASE 1,2
1.0T~2.5T
1.0T~2.5T
58.36MHz
17.135nS
0.5T
1.0T~2.5T
(c) DVD-R
±0.05T(2nS) STEP
26.16MHz
38.2263nS
1.0T~1.7T
0.3T~1.0T
(d) DVD-RW
±0.05T(2nS) STEP
TYPE 1,2
-0.35T~0.35T
0.5T
0.6T
0.2T~1.5T
0.15T~0.85T
0.4T
(e) DVD+RW
±0.05T(2nS) STEP
CAV/CLV
26.16MHz
38.2263nS
1T
0.3T~0.5T
(f) CD-RW 4X
±0.125T(7nS) STEP
17.2872MHz
56.8463nS
1T
0.5T

FIG. 4



BASE SETTING IS C_SFP[2..0]=3, C_EFP[2..0]=4, C_SMP[2..0]=3, C_SLP[2..0]=2, C_ELP[2..0]=3 and C_ELC[2..0]=4 FOR DVD−RAM

FIG. 5

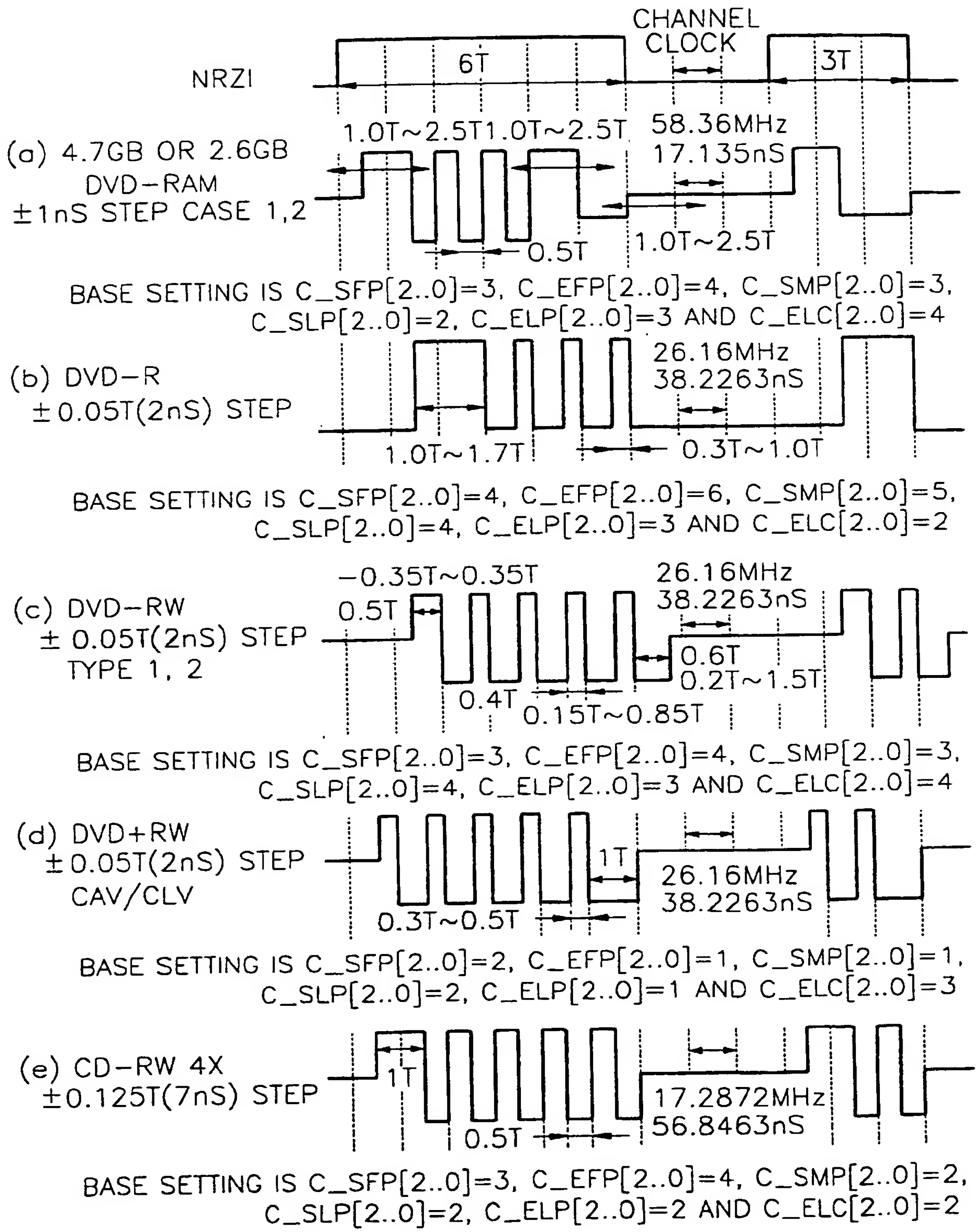

CHANNEL CLOCK
NRZI
6T
3T
(a) 4.7GB OR 2.6GB DVD-RAM ±1nS STEP CASE 1,2
1.0T~2.5T
1.0T~2.5T
58.36MHz
17.135nS
0.5T
1.0T~2.5T
BASE SETTING IS C_SFP[2..0]=3, C_EFP[2..0]=4, C_SMP[2..0]=3, C_SLP[2..0]=2, C_ELP[2..0]=3 AND C_ELC[2..0]=4
(b) DVD-R ±0.05T(2nS) STEP
26.16MHz
38.2263nS
1.0T~1.7T
0.3T~1.0T
BASE SETTING IS C_SFP[2..0]=4, C_EFP[2..0]=6, C_SMP[2..0]=5, C_SLP[2..0]=4, C_ELP[2..0]=3 AND C_ELC[2..0]=2
(c) DVD-RW ± 0.05T(2nS) STEP TYPE 1, 2
-0.35T~0.35T
0.5T
26.16MHz
38.2263nS
0.6T
0.2T~1.5T
0.4T
0.15T~0.85T
BASE SETTING IS C_SFP[2..0]=3, C_EFP[2..0]=4, C_SMP[2..0]=3, C_SLP[2..0]=4, C_ELP[2..0]=3 AND C_ELC[2..0]=4
(d) DVD+RW ±0.05T(2nS) STEP CAV/CLV
1T
26.16MHz
38.2263nS
0.3T~0.5T
BASE SETTING IS C_SFP[2..0]=2, C_EFP[2..0]=1, C_SMP[2..0]=1, C_SLP[2..0]=2, C_ELP[2..0]=1 AND C_ELC[2..0]=3
(e) CD-RW 4X ±0.125T(7nS) STEP
1T
17.2872MHz
56.8463nS
0.5T
BASE SETTING IS C_SFP[2..0]=3, C_EFP[2..0]=4, C_SMP[2..0]=2, C_SLP[2..0]=2, C_ELP[2..0]=2 AND C_ELC[2..0]=2

FIG. 6

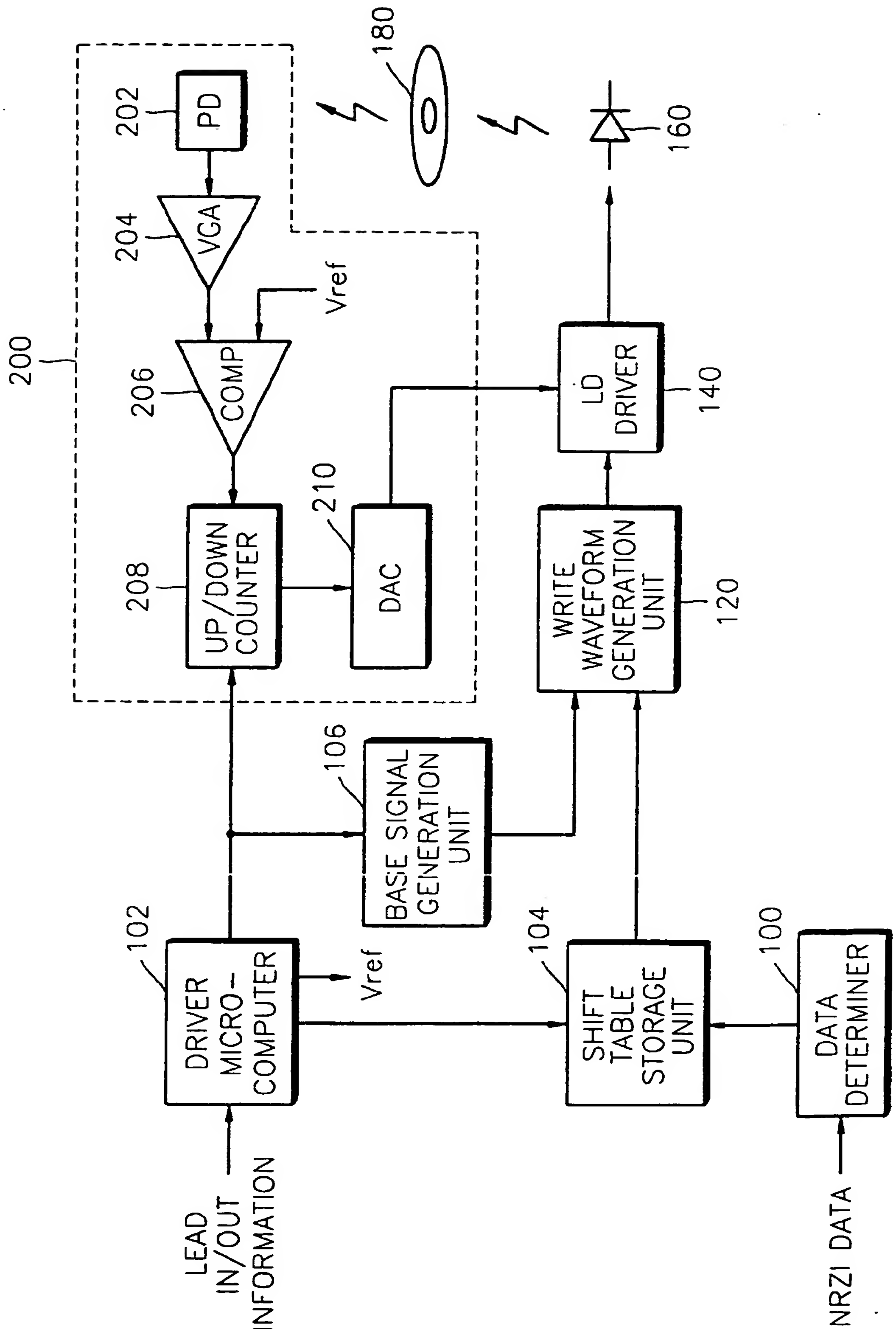

200
202
PD
204
VGA
206
COMP
Vref
208
UP/DOWN
COUNTER
210
DAC
180
160
LD
DRIVER
140
WRITE
WAVEFORM
GENERATION
UNIT
120
106
BASE SIGNAL
GENERATION
UNIT
102
DRIVER
MICRO-
COMPUTER
Vref
104
SHIFT
TABLE
STORAGE
UNIT
100
DATA
DETERMINER
LEAD
IN/OUT
INFORMATION
NRZI DATA

FIG. 7

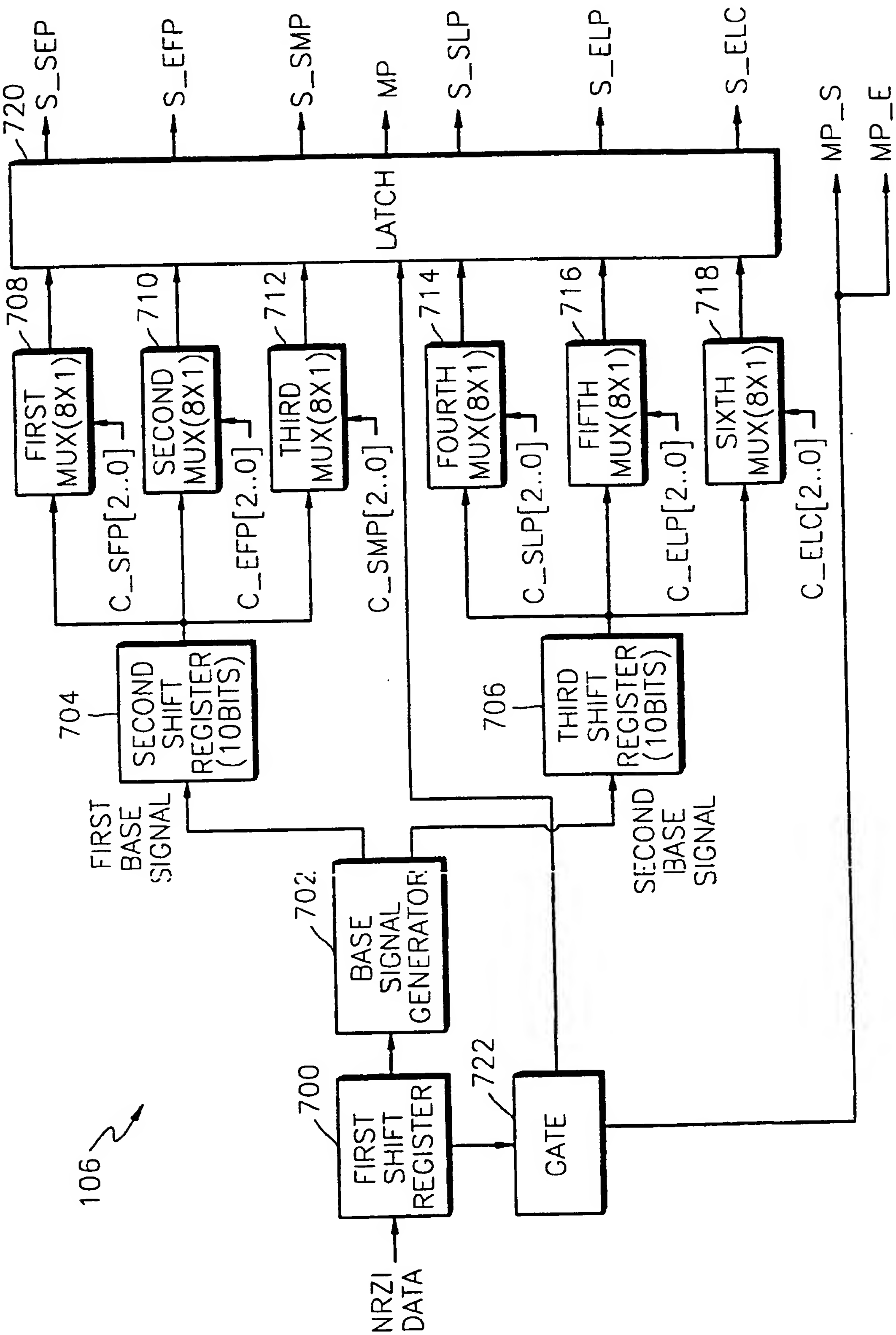
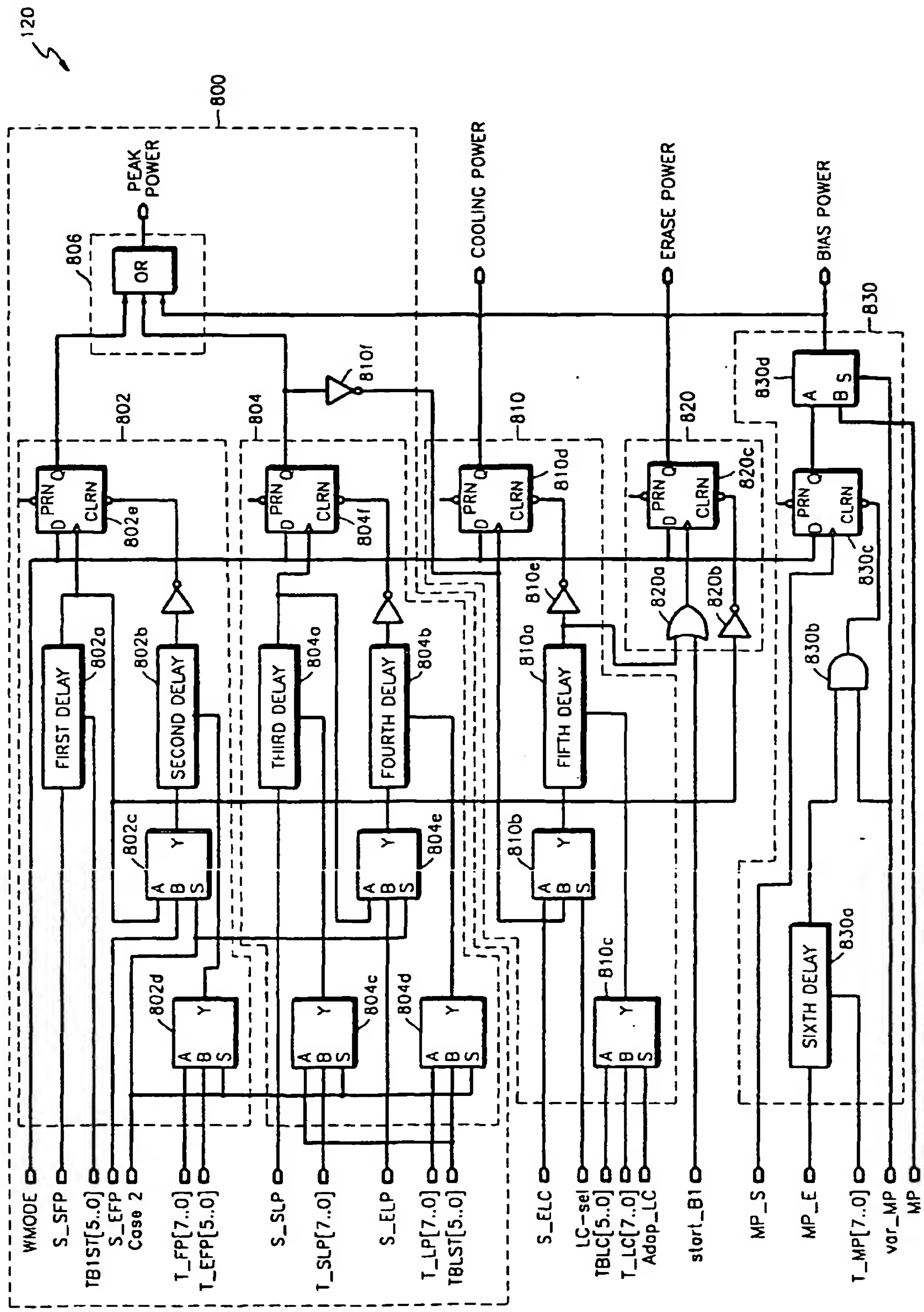

106
NRZI DATA
700
FIRST SHIFT REGISTER
702
BASE SIGNAL GENERATOR
722
GATE
FIRST BASE SIGNAL
SECOND BASE SIGNAL
704
SECOND SHIFT REGISTER (10BITS)
706
THIRD SHIFT REGISTER (10BITS)
708
FIRST MUX(8X1)
710
SECOND MUX(8X1)
712
THIRD MUX(8X1)
714
FOURTH MUX(8X1)
716
FIFTH MUX(8X1)
718
SIXTH MUX(8X1)
C_SFP[2..0]
C_EFP[2..0]
C_SMP[2..0]
C_SLP[2..0]
C_ELP[2..0]
C_ELC[2..0]
720
LATCH
S_SEP
S_EFP
S_SMP
MP
S_SLP
S_ELP
S_ELC
MP_S
MP_E

FIG. 8


120
800
PEAK POWER
806
OR
COOLING POWER
ERASE POWER
BIAS POWER
830
830d
810f
802
804
810
820
PRN
CLRN
802e
804f
810d
820c
830c
810e
820a
820b
830b
FIRST DELAY
SECOND DELAY
THIRD DELAY
FOURTH DELAY
FIFTH DELAY
SIXTH DELAY
802a
802b
804a
804b
810a
830a
802c
804e
810b
810c
802d
804c
804d
WMODE
S_SFP
TB1ST[5..0]
S_EFP
Case 2
T_FP[7..0]
T_EFP[5..0]
S_SLP
T_SLP[7..0]
S_ELP
T_LP[7..0]
TBLST[5..0]
S_ELC
LC-sel
TBLC[5..0]
T_LC[7..0]
Adap_LC
start_B1
MP_S
MP_E
T_MP[7..0]
var_MP
MP